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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/377,740	08/20/99	SHOJI K	32014-150502

EXAMINER	
CARROLL, J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/25/00

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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER NUMBER
	5

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined. ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire THREE (3) month(s), --- days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claim(s) 1 through 9 are pending in the application.
   Of the above, claim(s) _____ is withdrawn from consideration.
2. ☐ Claim(s) _____ has been canceled.
3. ☐ Claim(s) _____ is allowed.
4. ☒ Claim(s) 1 through 9 are rejected.
5. ☐ Claim(s) _____ is objected to.
6. ☐ Claim(s) _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawing(s) under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawing(s) are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction(s), filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☒ Acknowledgment is made of the claim for priority under 35 USC 119. The certified copy has ☒ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

The Official Draftsperson has objected to the Drawings as per Form PTO 948, enclosed herewith.

Claims 1 through 8 comply with the requirements of 35 U.S.C. 112.

Under 35 U.S.C. 103, we reject as unpatentable Claims 1, 2, 3, 4, 5, 6, 7 and 9 over considerations of presently cited and provided Ema, who referred to Aneha *et al.* (line 46, column 5) as demonstrating the usual, standard cell system. More particularly, Ema taught an integrated circuit and its method of manufacturing whereby the integrated circuit (Figure 7) comprised a plurality of basic cell functional blocks with predetermined function, *e.g.*, memory function, logic function, whereby the blocks were arranged in a line and accordingly interconnected (Figure 9) so as to achieve a desired function for implement the desired function. We thus conclude it to have been obvious for one to have readily achieved the claimed subject matter by simply following the expressed teachings and suggestions of Ema.

In re Claims 2, 3, 4 and 9, Ema anticipated using the standard cell system after Aneha *et al.*

In re Claim 7, Ema anticipated locating the basic cell function blocks within a central surface position of a semiconductor chip (Figures 4F, 5A, 5B, 7, 8F & 9).

Under 35 U.S.C. 103, we reject as unpatentable Claim 8 over the prior art information as applied *supra*, but further considered with presently cited and provided Kawashima indicating (Figures 1 through 3) that it was usual practice to have provided a second area of input/out buffers surrounding a first central area accommodating the basic cell functional blocks. We thus conclude it to have been usual and obvious thereby for one to have realized that the semiconductor integrated circuits disclosed by Ema inherently contained usual input/output buffers.

We reject all Claims.

An inquiry concerning this communication may be directed to Examiner J. Carroll at telephone number 703-308-4926 or, to the Reception Person for Technology Center 2800 at telephone number 703-308-0956. A written communication may be received in Art Unit 2811 at telefax number 703-308-7724.

Respectfully submitted.

James J. Carroll
Primary Examiner